SC1544
ACPI Controller for Advanced Motherboards

Description

Semtech's SC1544, SC243x and SC1112A or SC1114 provide all the voltages necessary for an ACPI system.

The SC1544 offers five independant supplies: a 5V dual supply for USB, a 3.3V dual supply for PCI, a 3.3V or 2.5V dual supply for memory, a 1.5V or 3.3V supply for AGP and a 1.8V supply. The AGP supply is programmble using the system TYPEDET signal.

An on-board internal charge pump eliminates the need for P-channel MOSFETs and enables function from a single 5V supply (system 5VSB). All dual outputs are over current protected.

The SC1544 differs from the SC1547 in three important ways: 1) the device initially starts up in S5, and not G0 like the SC1547; 2) the gate drives for the 1.8V and AGP outputs are always high in normal operation; 3) no OCP on the 1.8V and AGP outputs.

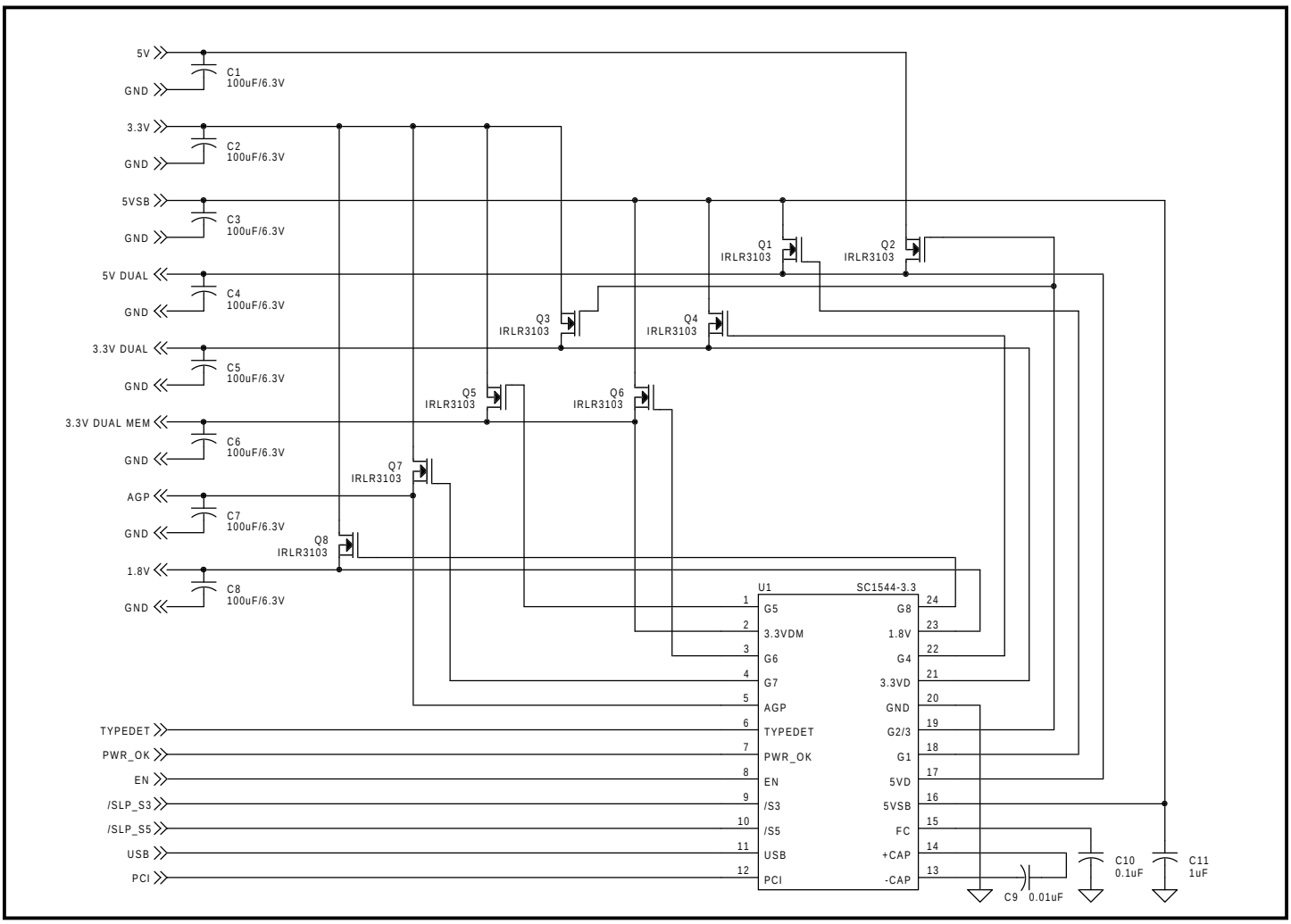
Features

- Complete programmable supply for instantly available PC systems
- Supports 2.5V memory or 3.3V memory (-2.5 or -3.3 option in part number)
- 5V dual and 3.3V dual supplies are programmable to be active or inactive in S5
- Integrated AGP voltage supply with "TYPEDET" signal for 3.3V or 1.5V operation
- Integrated LDO for 1.8V supply
- Integrated charge pump removes the need for PMOS FETs, enables single supply operation
- Over current protection on all dual outputs
- Inherent soft-start capability
- TSSOP-24 package

Applications

- Instantly available motherboards

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{5VSB}	-0.6 to 7	V
Logic Input Pins		-0.6 to V_{5VSB}	V
Charge Pump Output Voltage	V_{FC}	-0.6 to 13.2	V
Thermal Impedance Junction to Case	θ_{JC}	15.6	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	83.8	°C/W
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature Range	T_J	0 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics(1)

Unless specified: all applicable silver box supplies (3.3V, 5V, 5VSB) ± 5%, GND = 0V, $V_{SENSE\ PINS} = V_{OUT(NOM)}$, T_A = 25°C. Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
IN						
Supply Voltage	V_{5VSB}		**4.5**	5.0	**5.5**	V
Quiescent Current	I_Q	All states (S0, S3, S5, disabled)		10	15	mA
					20	
Undervoltage Lockout						
Threshold Voltage	V_{UVLO}	V_{5VSB} Rising	**3.5**	4.0	**4.4**	V
Logic Inputs (EN, PCI, PWR_OK, /S3, /S5, TYPEDET, USB)						
Logic Pin Sink Current(2)	I_{SINK}	V_{BIAS} = 5V, all logic pins		0.1	**1**	µA
Logic Pin Source Current	I_{SOURCE}	EN, V_{EN} = 0V		0.5	**3**	µA
		PCI, TYPEDET, USB, V_{PIN} = 0V		50	**200**	
		/S3, PWR_OK, V_{PIN} = 0V		100	**400**	
		/S5, $V_{/S5}$ = 0V		150	**600**	
Threshold Voltage	V_{IH}		**2.4**			V
	V_{IL}				**0.8**	V
1.8V Output						
Output Voltage(3)	$V_{1.8V}$	1mA ≤ I_{OUT} ≤ 720mA	1.764	1.800	1.836	V
			1.746		**1.854**	

Electrical Characteristics (Cont.)(1)

Unless specified: all applicable silver box supplies (3.3V, 5V, 5VSB) ± 5%, GND = 0V, $V_{SENSE\ PINS} = V_{OUT(NOM)}$, T_A = 25°C. Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
1.8V Output (Cont.)						
Line Regulation(3)	REG_{LINE}	V_{5VSB} = 4.75V to 5.25V, I_{OUT} = 0A		0.01	**0.10**	%
Load Regulation(3)	REG_{LOAD}	V_{5VSB} = 5V, I_{OUT} = 0A to 720mA		0.01	**0.20**	%
Gate 8 Drive Voltage(4)	$V_{G8(HI)}$	$V_{1.8V}$ = 1.7V, I_{G8} = 10µA	**8.00**	8.75		V
	$V_{G8(LO)}$	S3, I_{G8} = -10µA		0.8	**1.0**	
Gate 8 Drive Current(4)	$I_{G8(SOURCE)}$	$V_{1.8V}$ = 1.7V, V_{G8} = 5V	**2**	4		mA
	$I_{G8(SINK)}$	$V_{1.8V}$ = 1.9V, V_{G8} = 3V	**-3.5**	-5		
Sense Pin Bias Current	$I_{1.8V}$	Sinking, $V_{1.8V}$ = 1.8V	**-70**	-100	**-130**	µA
2.5V/3.3V Dual Memory Output						
Output Voltage(5)	$V_{3.3VDM}$	1mA ≤ I_{OUT} ≤ 720mA	-1.5	$V_{OUT(NOM)}$	+1.5	%
			-2.5		**+2.5**	
Line Regulation(5)	REG_{LINE}	V_{5VSB} = 4.75V to 5.25V, I_{OUT} = 0A		0.01	**0.10**	%
Load Regulation(5)	REG_{LOAD}	V_{5VSB} = 5V, I_{OUT} = 0A to 720mA		0.01	**0.20**	%
Gate 5 Drive Voltage(6)	$V_{G5(HI)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ - 100mV, I_{G5} = 10µA, S0	**8.00**	8.75		V
	$V_{G5(LO)}$	I_{G5} = -10µA, S3		0.8	**1.0**	
Gate 5 Drive Current(6)	$I_{G5(SOURCE)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ - 100mV, V_{G5} = 5V, S0	**2**	4		mA
	$I_{G5(SINK)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ + 100mV, V_{G5} = 3V, S0	**-3.5**	-5		
Gate 6 Drive Voltage(7)	$V_{G6(HI)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ - 100mV, I_{G6} = 10µA, S3	**8.00**	8.75		V
	$V_{G6(LO)}$	I_{G6} = -10µA, S0		0.8	**1.0**	
Gate 6 Drive Current(7)	$I_{G6(SOURCE)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ - 100mV, V_{G6} = 5V, S3	**2**	4		mA
	$I_{G6(SINK)}$	$V_{3.3VDM} = V_{OUT(NOM)}$ + 100mV, V_{G6} = 3V, S3	**-3.5**	-5		
Sense Pin Bias Current	$I_{3.3VDM}$	Sinking, 3.3V option, $V_{3.3VDM}$ = 3.3V	**-330**	-475	**-620**	µA
		Sinking, 2.5V option, $V_{3.3VDM}$ = 2.5V	**-215**	-310	**-405**	
3.3V Dual Output						
Output Voltage(8)	$V_{3.3VD}$	1mA ≤ I_{OUT} ≤ 720mA	3.250	3.300	3.350	V
			3.217		**3.383**	
Line Regulation(8)	REG_{LINE}	V_{5VSB} = 4.75V to 5.25V, I_{OUT} = 0A		0.01	**0.10**	%
Load Regulation(8)	REG_{LOAD}	V_{5VSB} = 5V, I_{OUT} = 0A to 720mA		0.01	**0.20**	%

Electrical Characteristics (Cont.)(1)

Unless specified: all applicable silver box supplies (3.3V, 5V, 5VSB) ± 5%, GND = 0V, $V_{SENSE\ PINS} = V_{OUT(NOM)}$, T_A = 25°C. Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
3.3V Dual Output (Cont.)						
Gate 3 Drive Voltage(9)	$V_{G3(HI)}$	I_{G3} = 10µA	**8.00**	8.75		V
	$V_{G3(LO)}$	I_{G3} = -10µA		40	**100**	mV
Gate 3 Drive Current(9)	$I_{G3(SOURCE)}$	V_{G3} = 5V	**0.5**	0.7		mA
	$I_{G3(SINK)}$	V_{G3} = 3V	**-10**	-14		
Gate 4 Drive Voltage(10)	$V_{G4(HI)}$	$V_{3.3VD}$ = 3.2V, I_{G4} = 10µA	**8.00**	8.75		V
	$V_{G4(LO)}$	$V_{3.3VD}$ = 3.4V, I_{G4} = -10µA		0.8	**1.0**	
Gate 4 Drive Current(10)	$I_{G4(SOURCE)}$	$V_{3.3VD} = V_{OUT(NOM)}$ - 100mV, V_{G4} = 5V	**2**	4		mA
	$I_{G4(SINK)}$	$V_{3.3VD} = V_{OUT(NOM)}$ + 100mV, V_{G4} = 3V	**-3.5**	5		
Sense Pin Bias Current	$I_{3.3VD}$	Sinking, $V_{3.3VD}$ = 3.3V	**-70**	-100	**-130**	µA
5V Dual Output						
Gate 2 Drive Voltage(11)	$V_{G2(HI)}$	I_{G2} = 10µA	**8.00**	8.75		V
	$V_{G2(LO)}$	I_{G2} = -10µA		40	**100**	mV
Gate 2 Drive Current(11)	$I_{G2(SOURCE)}$	V_{G2} = 5V	**0.5**	0.7		mA
	$I_{G2(SINK)}$	V_{G2} = 3V	**-10**	-14		
Gate 1 Drive Voltage(12)	$V_{G1(HI)}$	I_{G1} = 10µA	**8.00**	8.75		V
	$V_{G1(LO)}$	I_{G1} = -10µA		40	**100**	mV
Gate 1 Drive Current(12)	$I_{G1(SOURCE)}$	V_{G1} = 5V	**0.5**	0.7		mA
	$I_{G1(SINK)}$	V_{G1} = 3V	**-10**	-14		
Sense Pin Bias Current(2)	I_{5VD}	V_{5VD} = 5V			**16**	µA
AGP Output						
Output Voltage(13)	V_{AGP}	1mA ≤ I_{OUT} ≤ 720mA	-2.0	$V_{OUT(NOM)}$	+2.0	%
			-3.0		**+3.0**	
Line Regulation(13)	REG_{LINE}	V_{5VSB} = 4.75V to 5.25V, I_{OUT} = 0A		0.01	**0.10**	%
Load Regulation(13)	REG_{LOAD}	V_{5VSB} = 5V, I_{OUT} = 0A to 720mA		0.01	**0.20**	%
Gate 7 Drive Voltage(4)	$V_{G7(HI)}$	$V_{AGP} = V_{OUT(NOM)}$ - 100mV, I_{G7} = 10µA	**8.00**	8.75		V
	$V_{G7(LO)}$	$V_{AGP} = V_{OUT(NOM)}$ + 100mV, I_{G7} = -10µA		0.8	**1.0**	V

Electrical Characteristics (Cont.)(1)

Unless specified: all applicable silver box supplies (3.3V, 5V, 5VSB) ± 5%, GND = 0V, $V_{SENSE\ PINS} = V_{OUT(NOM)}$, T_A = 25°C. Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
AGP Output (Cont.)						
Gate 7 Drive Current(4)	$I_{G7(SOURCE)}$	$V_{AGP} = V_{OUT(NOM)}$ - 100mV, V_{G7} = 5V	**2**	4		mA
	$I_{G7(SINK)}$	$V_{AGP} = V_{OUT(NOM)}$ + 100mV, V_{G7} = 3V	**-3.5**	-5		
Sense Pin Bias Current	I_{AGP}	V_{AGP} = 3.3V, TYPEDET = High	**-235**	-340	**-445**	µA
		V_{AGP} = 1.5V, TYPEDET = Low	**-70**	-105	**-140**	
FC (Charge Pump)						
Output Voltage	V_{FC}	V_{5VSB} = 5V	**9.0**	9.5	**10.0**	V
Overcurrent Protection(14)						
Trip Threshold	$V_{TH(OC)}$		**30**	50	**70**	$\%V_{OUT}$
Short Circuit Immunity(15)			1		75	ms

Notes:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

(2) Guaranteed by design.

(3) Applies to S0 only.

(4) Gates 7 and 8 are high whenever 5VSB is present and greater than V_{UVLO}, unless the over current protection has been tripped.

(5) Applies to S3 sleep state only for 3.3V Dual Memory option. Applies to both S0 and S3 sleep state for 2.5V Dual Memory Option

(6) Gate 5 is high in S0 and low in the S3 and S5 sleep states.

(7) Gate 6 is high in the S3 sleep state and low in S0 and in the S5 sleep state.

(8) Applies to S3 sleep state and S5 sleep state when the PCI pin is high.

(9) Gate 3 is high in S0 and low in the S3 and S5 sleep states.

(10) Gate 4 is high in the S3 sleep state and the S5 sleep state when the PCI pin is high. Gate 4 is low in S0, and in the S5 sleep state when the PCI pin is low.

(11) Gate 2 is high in S0 and low in the S3 and S5 sleep states.

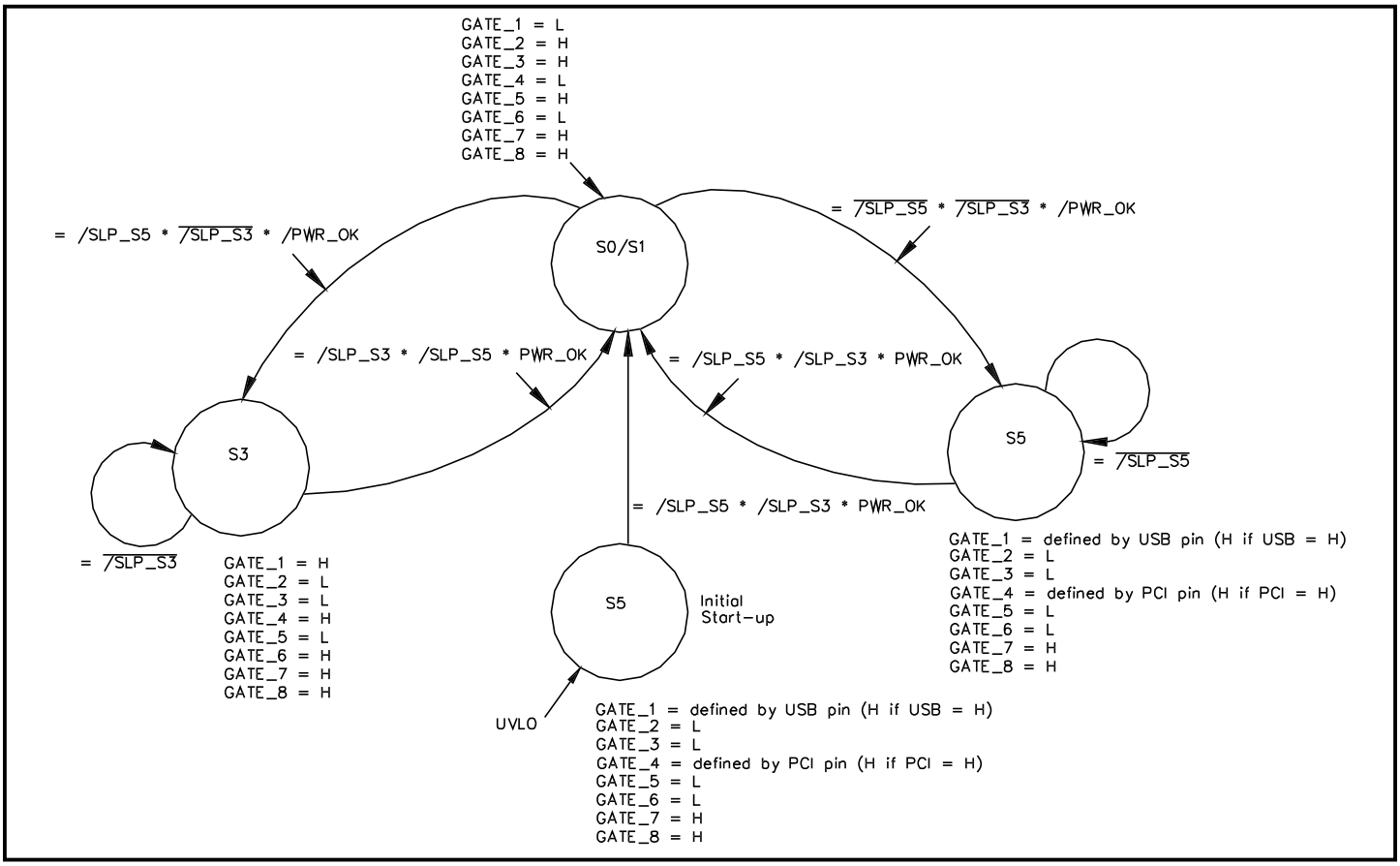
(12) Gate 1 is high in the S3 sleep state and the S5 sleep state when the USB pin is high. Gate 1 is low in S0, and in the S5 sleep state when the USB pin is low.

(13) Applies to S0 only. V_{AGP} = 3.3V when TYPEDET is high and 1.5V when the TYPEDET pin is low.

(14) Applies to 2.5V/3.3V Dual Memory, 3.3V Dual and 5V Dual outputs when enabled only. When an output is disabled, that output is not monitored for OCP. The 1.8V and AGP outputs do not have over current protection.

(15) Minimum and maximum time limits for over current protection to trip when powered up (or enabled) into a shorted output and when a short is applied to an enabled, OCP protected output.

State Diagram Showing Gate Drive Status

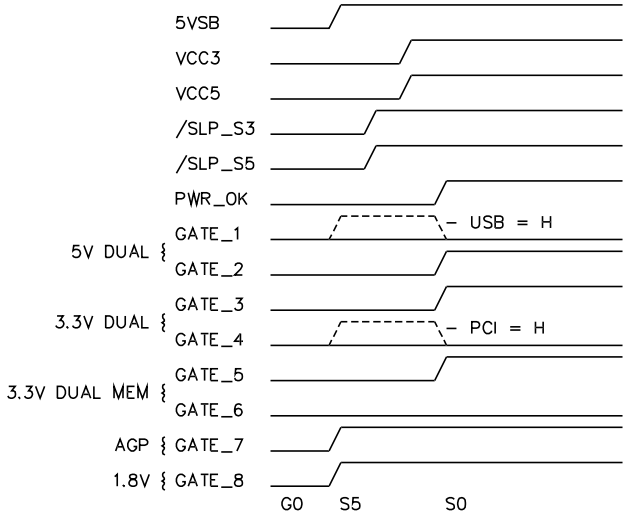


Note:

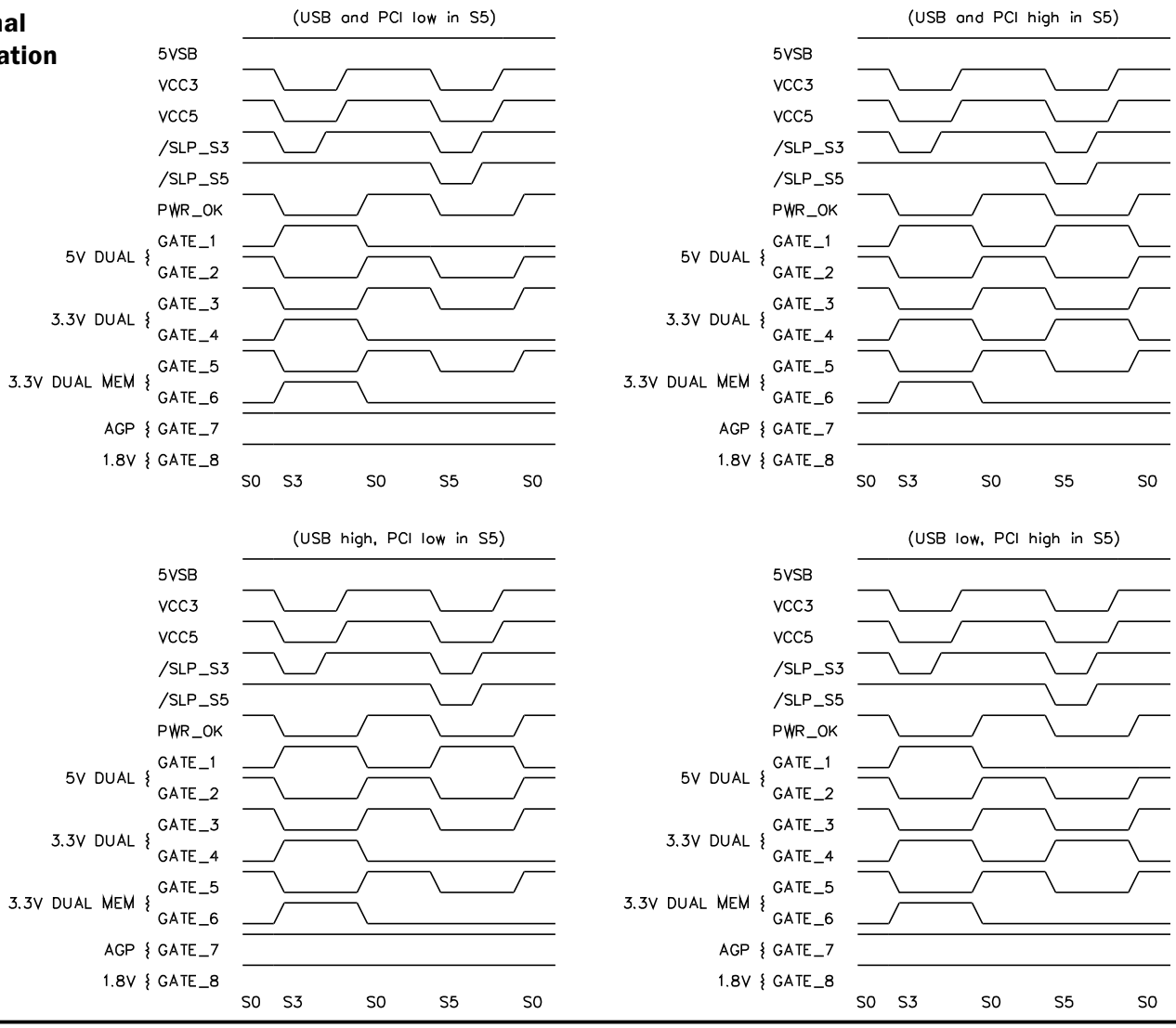
(1) State machine will not allow illegal transitions such as S3 to S5. In order to get to S5 from S3, it is first necessary to enter S0.

Timing Diagrams

Startup



Normal Operation



Power Matrix

This table shows which output is powered from which supply under each system state.

System State	USB	PCI	/S3	/S5	PWR_OK	3.3V/2.5V Dual Memory	3.3V Dual	5V Dual	3.3V/1.5V AGP(2)	1.8V(2)	Comments
S0	X(1)	X(1)	1	1	1	3.3V	3.3V	5V	3.3V	3.3V	
S3	X(1)	X(1)	0	1	0	5VSB	5VSB	5VSB	ON	ON	
S5	0	0	0	0	0	OFF	OFF	OFF	ON	ON	All outputs off
	0	1	0	0	0	OFF	5VSB	OFF	ON	ON	PCI enabled
	1	0	0	0	0	OFF	OFF	5VSB	ON	ON	USB enabled
	1	1	0	0	0	OFF	5VSB	5VSB	ON	ON	PCI & USB enabled

Notes:

(1) X = "don't care". In S0 and S3, the 3.3V dual and 5V dual outputs are not affected by the state of the PCI and USB pins. These outputs are only controlled by the sate of the PCI and USB pins in S5.

(2) Gate 7 and Gate 8 are high in all states with 5VSB > UVLO and OCP not tripped. If powered from 3.3V as shown in the table, the AGP and 1.8V outputs are only present in S0, and will ramp with the 3.3V supply as it comes up. This avoids dips in the 3.3V supply which would otherwise occur if Gate 7 and Gate 8 went high after the 3.3V supply came up, demanding high currents to charge output capacitors. If powered from 5VSB they can be used to create 1.5VSB, 1.8VSB or 3.3VSB as required.

Gates At A Glance

This table shows which gate drive pin controls which MOSFET:

Gate Number:	Pin Number:	Drives the FET between:			FET mode:
1	18	5VSB	and	5V Dual	pass device
2	19(1)	5V		5V Dual	pass device
3	19(1)	3.3V		3.3V Dual	pass device
4	22	5VSB		3.3V Dual	linear regulator
5	1	3.3V		3.3V/2.5V Dual Memory	pass device/linear regulator(2)
6	3	5VSB		3.3V/2.5V Dual Memory	linear regulator
7	4	3.3V		AGP	linear regulator
8	24	3.3V		1.8V	linear regulator

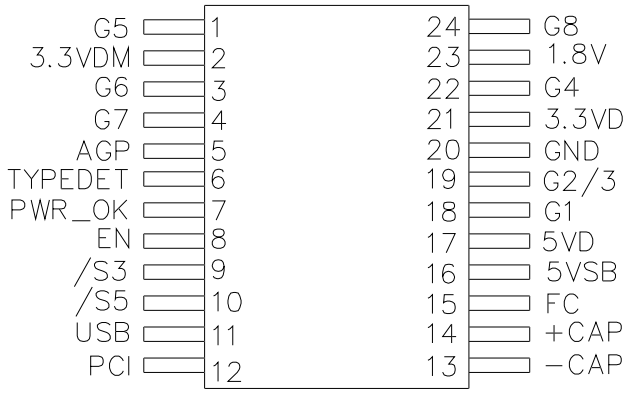
Notes:

(1) Note common pin for Gate 2 and Gate 3 - both FETs are operating as pass devices only in S0.

(2) FET is acting as a pass device for 3.3V Dual Memory and as a linear regulator for 2.5V Dual Memory.

Pin Configuration

Top View



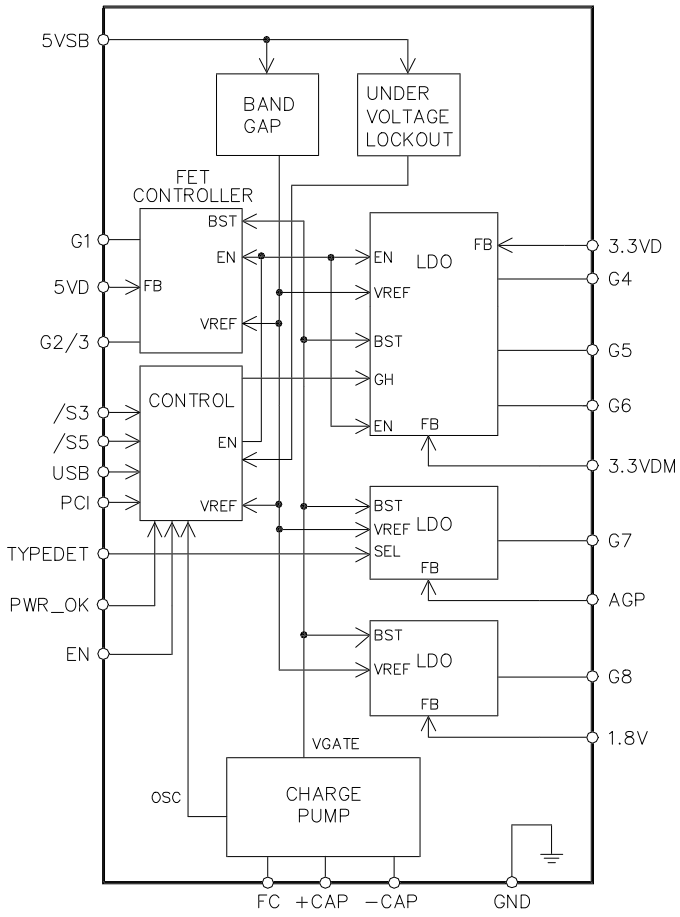
TSSOP-24

Ordering Information

Part Number	Package
SC1544TS-X.XTR (1)(2)	TSSOP-24
SC1544EVB(3)	N/A

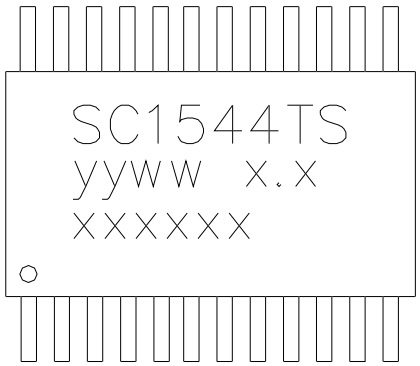
Notes:
(1) Where -X.X denotes voltage options. Available voltages are: 2.5V and 3.3V (2.5V Dual Memory or 3.3V Dual Memory).
(2) Only available in tape and reel packaging. A reel contains 2500 devices.
(3) Evaluation board for SC1544 - specify voltage option when ordering.

Block Diagram



Marking Information

Top View

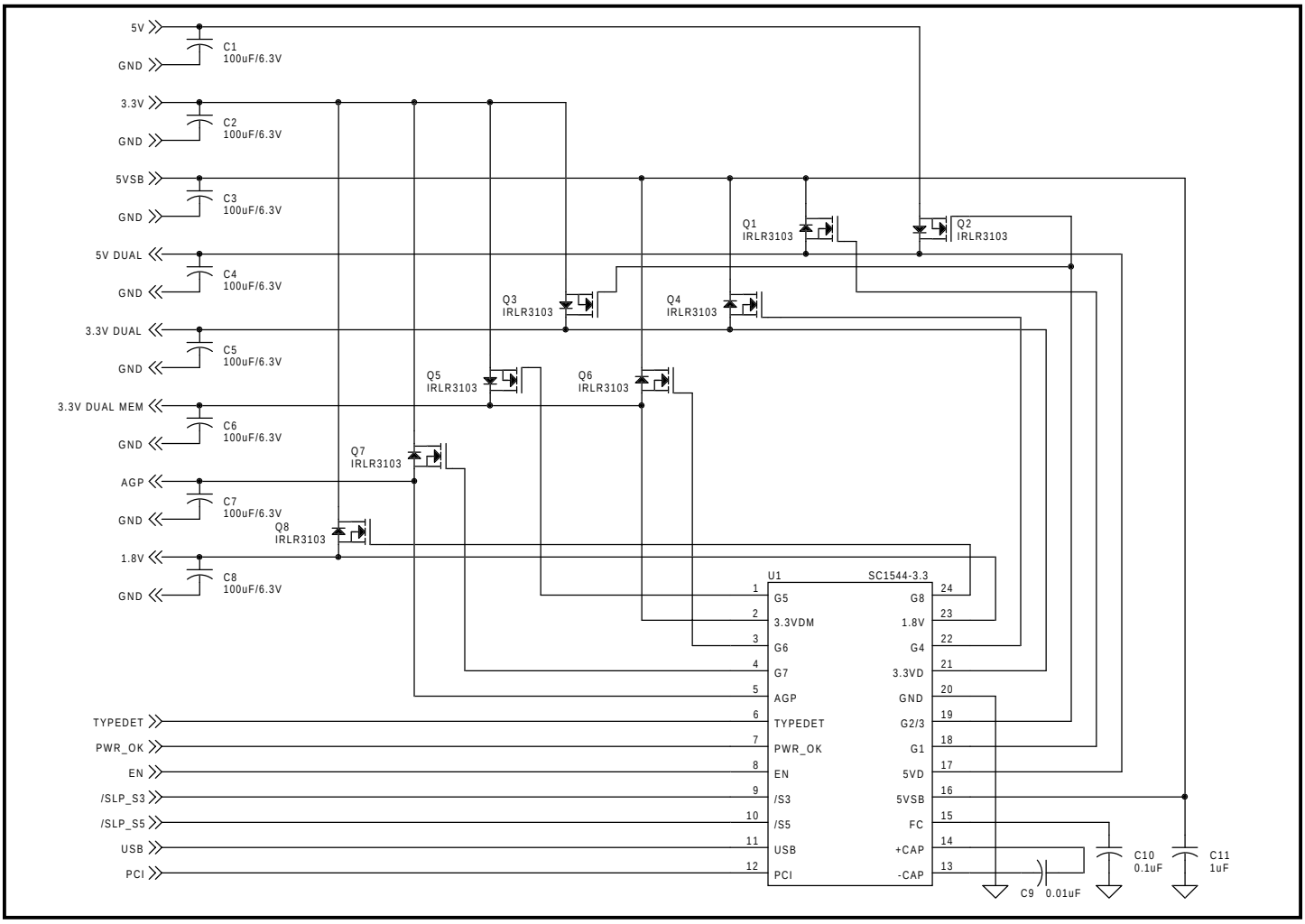


x.x = voltage option (Example: 3.3)
yyww = Date code (Example: 0012
xxxxxx = Lot number (Example: P94A01)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	G5	Gate drive for MOSFET between VCC3 and 2.5V/3.3V Dual Memory.
2	3.3VDM	Sense pin for 3.3V Dual Memory. Sense pin for 2.5V Dual Memory for 2.5V option.
3	G6	Gate drive for MOSFET between 5VSB and 2.5V/3.3V Dual Memory.
4	G7	Gate drive for MOSFET between VCC3 and 1.5V/3.3V AGP. High when 5VSB is present and greater than UVLO.
5	AGP	Sense pin for 1.5V/3.3V AGP.
6	TYPEDET	Select 1.5V or 3.3V for AGP, high = 3.3V.
7	PWR_OK	Power_OK signal from silver box.
8	EN	Enable signal active high. Connect to 5VSB if not being used. Cycling the enable pin will reset the over current latches.
9	/S3	Pulling this pin low (with /S5 high) causes the device to enter the S3 sleep state. Pulling both /S3 and /S5 low will cause the device to enter the S5 sleep state.
10	/S5	Pulling this pin low along with /S3 causes the device to enter the S5 sleep state.
11	USB	Enable pin for 5V Dual during S5 sleep state, high = ON.
12	PCI	Enable pin for 3.3V Dual during S5 sleep state, high = ON.
13	-CAP	Negative end of charge pump capacitor. Connect a 10nF ceramic capacitor between this pin and pin 14 (+CAP).
14	+CAP	Positive end of charge pump capacitor.
15	FC	Charge pump output (9V nominal). Decouple this pin with a 0.1µF ceramic capacitor.
16	5VSB	5V standby supply from silver box. Decouple this pin with a 1µF ceramic capacitor.
17	5VD	Sense pin for 5V Dual.
18	G1	Gate drive for MOSFET between 5VSB and 5V Dual.
19	G2/3	Gate drive for MOSFETs between VCC5 and 5V Dual and VCC3 and 3.3V Dual.
20	GND	Reference ground.
21	3.3VD	Sense pin for 3.3V Dual.
22	G4	Gate drive for MOSFET between 5VSB and 3.3V Dual.
23	1.8V	Sense pin for 1.8V LDO.
24	G8	Gate drive for MOSFET between VCC3 (or 5VSB) and 1.8V. High when 5VSB is present and greater than UVLO.

Typical Applications Circuits

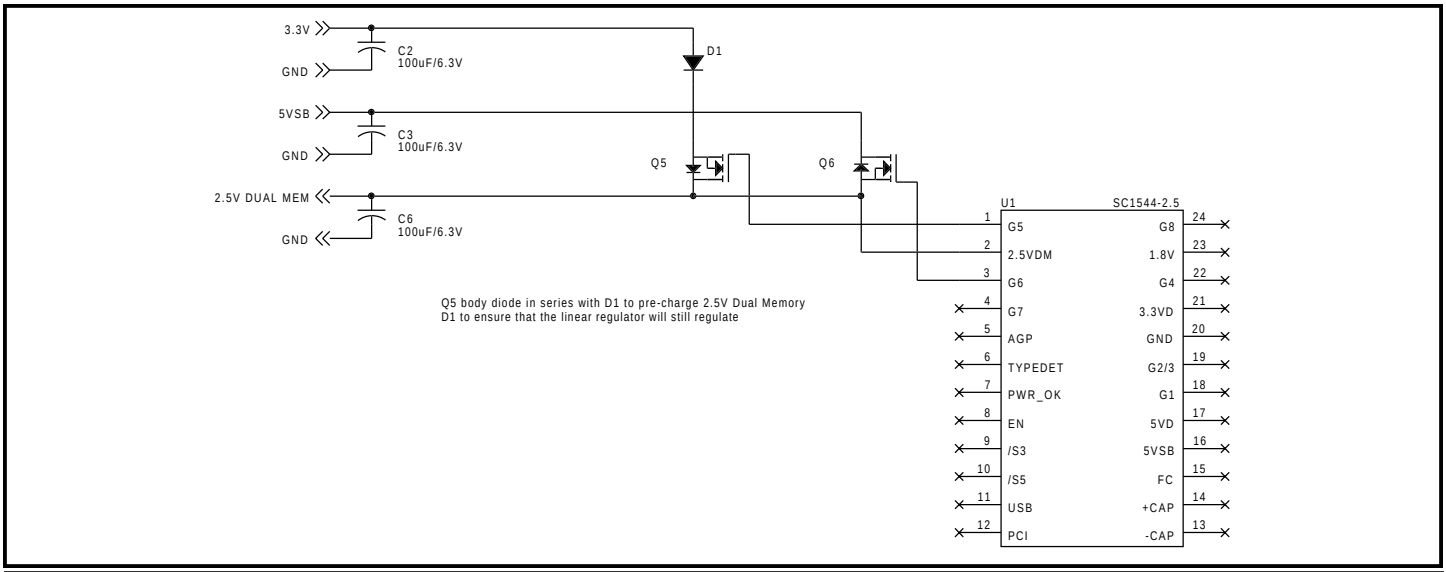


Notes:

(1) 3.3V option shown - see below for Q5 configuration for 2.5V option.

(2) 1.8V output shown powered from 3.3V. If powered from 5VSB, this becomes 1.8VSB.

(3) See Applications Information.



Applications Information

Theory Of Operation

The SC1544 provides a simple way to power five seperate voltage buses while controlling them correctly using the ACPI control interface (PWR_OK, /SLP_S3 and /SLP_S5).

It requires only a single supply rail (5VSB from the system silver box) to operate. An internal charge pump generates the gate voltages required to enable the use of n-channel FETs throughout the design. The external FETs are operated in two discrete modes:
1) as pass devices where $V_{OUT} = V_{IN} - (I_{OUT} * R_{DS(ON)})$
2) as linear regulators.
Please refer to the "Gates At A Glance" section on page 8 and the Typical Applications Circuits on page 11 to determine which FETs operate in which mode.

Linear Mode: the SC1544 contains a bandgap reference trimmed for optimal temperature coefficient which is fed into the inverting input of an error amplifier. The output voltage of each linear regulator (monitored by the sense pin for that output) is divided down internally using a resistor divider and compared to the bandgap voltage. The error amplifier drives the gate of the appropriate external FET to maintain the voltage at the non inverting input, and hence the output voltage.

Pass Device Mode: when a particular output is enabled (please refer to the "Power Matrix" section on page 8) in pass mode (i.e. 5VSB to 5V Dual), the appropriate gate drive will be driven high to turn the FET hard on, minimizing the voltage drop due to $I_{OUT}*R_{DS(ON)}$.

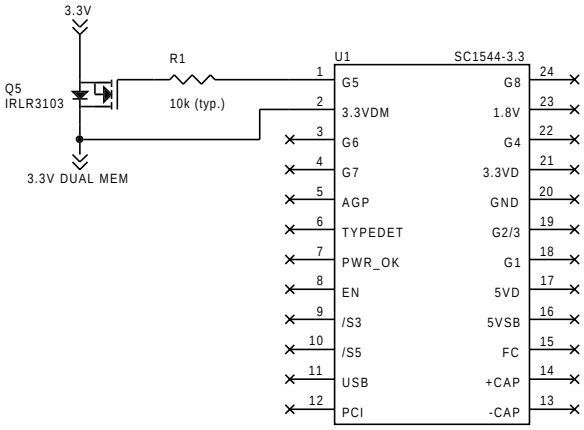
The **sense pins** serve two functions:
1) to sense the output voltage for the linear regulators
2) to sense the output voltage for over current protection

Over Current Protection is provided for all dual outputs. OCP is implemented by utilizing the $R_{DS(ON)}$ of the FETs. As the output current increases, the regulation loop maintains the output voltage (linear mode only) by turning on the FET more and more. Eventually, as the $R_{DS(ON)}$ low limit is reached (pass devices are already operating at this point) the FET will be unable to turn on any further and the output voltage will start to fall. When the output voltage falls to approximately 50% of nominal, all outputs are latched off. Toggling the enable pin or cycling 5VSB will reset the latch.

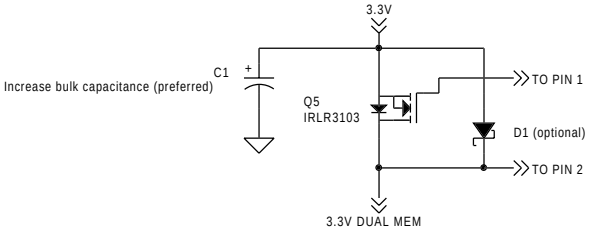
To prevent false latching due to capacitor inrush currents, low supply rails or momentary overloads, the current limit latch has a timer. If V_{OUT} is above the OCP threshold ($V_{TH(OC)}$) before the timer "times out", then the outputs do not latch.

Reducing Commutation Noise

The slew rate of the linears is slow enough to provide soft commutation. The non-linear switch outputs (5V and 3.3V Duals) have fast slew rates. It may be necessary to put a resistor in series with the gate to reduce transients (3.3V Dual Memory shown):



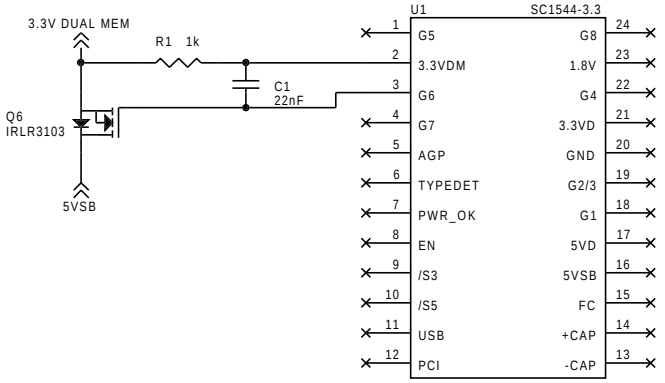
Another possible source of commutation noise occurs at startup on 3.3V Dual Memory, when the standby FET, Q6 and the pass-through FET, Q5 are both off. 3.3V Dual Memory will charge to 3.3V minus 0.7V (the drop across the Q5 body diode). When PWR_OK asserts, Q6 turns on shorting 3.3V to 3.3V Dual Memory, pulling it down locally momentarily. This should not be an issue as long as there is sufficient capacitance on 3.3V locally. Another way to reduce this drop is to place a schottky diode across Q5 with the cathode towards 3.3V Dual Memory so this rail charges to 3.3V minus 0.4V, thus reducing the drop when Q5 turns on:



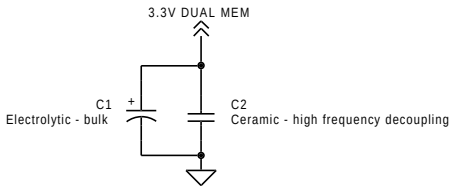
Applications Information (Cont.)

Linear Regulator Stability

When extremely low ESR capacitors (Oscons, Polymers, high value ceramics) are used on outputs requiring fast transients (3.3V/2.5V memory), the linear regulators may exhibit some overshoot and/or transient instability. External compensation may be necessary (5VSB to 3.3V Dual Memory shown):



Another possibility is to use dual capacitor types for the load capacitor - a ceramic capacitor will provide high frequency decoupling for the load while an electrolytic capacitor (high ESR) will tame the Q to prevent instability:



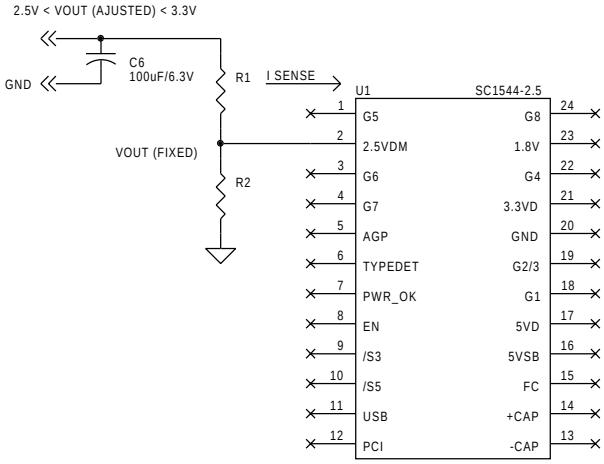
Adjusting the Output Voltage of the Linear Regulators

It is possible to adjust the output voltage of the linear regulators (1.8V, 2.5V Dual Memory and AGP) by applying an external resistor divider to the sense pin (see below). Since the sense pins sink a nominal 100µA (1.8V LDO, 150µA for the 1.5V AGP LDO, 325µA for the 3.3V AGP LDO and 350µA for the 2.5V Dual Memory LDO), the resistor values should be selected to allow 100x that current to flow through the divider. This will ensure that variations in the sense current will have negligible affect on the output voltage regulation. Thus a target value for R2 (maximum) can be calculated:

$$R2 \le \frac{V_{OUT(FIXED)}}{I_{SENSE} \bullet 100} \quad \Omega$$

For the 2.5V Dual Memory linear regulator:

$$R2 \le \frac{2.5}{350\mu A \bullet 100} \quad \le 71\Omega$$



The output voltage can only be adjusted upwards from the fixed output voltage, and can be calculated using the following equation:

$$V_{OUT(ADJUSTED)} = V_{OUT(FIXED)} \bullet \left(1 + \frac{R1}{R2}\right) + R1 \bullet I_{SENSE} \text{ Volts}$$

Therefore to set the 2.5V Dual Memory linear regulator to 2.6V, for example, R1 = 2.8Ω and R2 = 69.8Ω. The maximum voltage to which an output can be set using this method is limited by the input voltage to the FET(s) and the $R_{DS(ON)}$ of the FET(s).

Please note that this technique cannot be used for the 3.3V Dual Memory, 3.3V Dual and 5V Dual outputs since the output is switched via a pass device (i.e. not regulated) when not in S0.

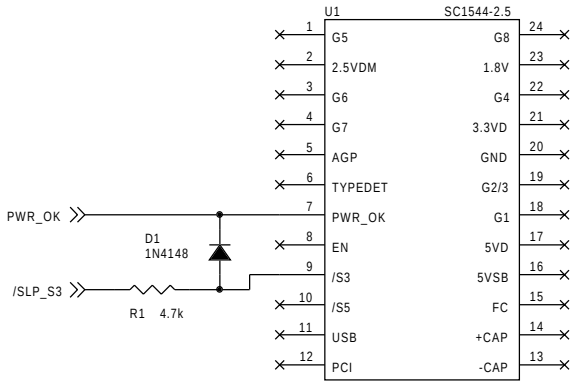
Fault Protection Hints

Loss of AC Power: if it is possible during brownouts or momentary loss of AC power to the computer “silver box” that PWR_OK can assert low while S3 and S5 remain high then the over current protection may trigger. This is because the state machine will ignore this illegal transition and monitor all outputs as if they are still in S0, despite the fact that the inputs are going away. If 5VSB decays slowly, S3 and S5 remain high, and one output drops below the OCP threshold for long enough

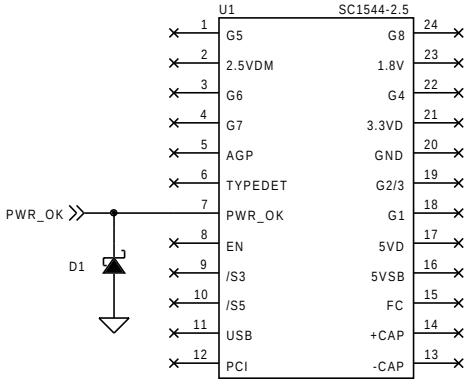
Applications Information (Cont.)

Fault Protection Hints (Cont.)

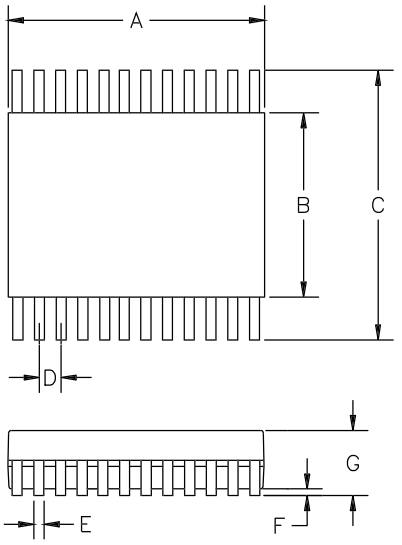
that the OCP "times out" then the outputs will latch off. Then if the AC power returns after the OCP latches off, but before the 5VSB supply drops below UVLO, then the device will not start up again until EN or 5VSB is cycled. One way to avoid this happening is to force the device into S3 if PWR_OK goes low but S3 and S5 remain high using the circuit shown below. This will supply the outputs from 5VSB which will either cause 5VSB to drop below UVLO and reset the part when the AC power comes back up, or it may prevent OCP occuring at all. Either way correct functionality will be guaranteed once AC power returns.

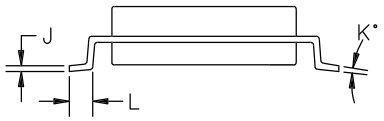


Incorrect Signals From Silver Box: Some silver boxes have been found that produce incorrect voltages on the PWR_OK line, producing dangerous negative voltage spikes up to -1V or greater. Such spikes exceed the absolute maximum ratings for this device and can cause the device to malfunction. If a supply produces such spikes they can be clamped to GND using a small schottky diode as shown below, completely removing any threat.



Outline Drawing - TSSOP-24





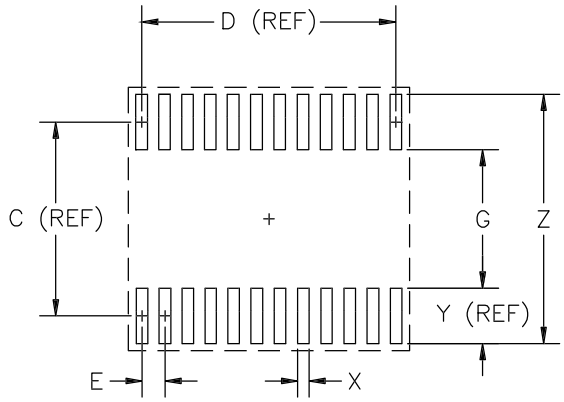
DIMENSIONS ①					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3031	.3110	7.70	7.90	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AD

② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

① CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-24



DIMENSIONS ①					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.282	—	7.15	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	REF
Y	—	.062	—	1.583	—
Z	—	.280	—	7.113	—

② GRID PLACEMENT COURTYARD IS 16 X 15 ELEMENTS (8mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

① CONTROLLING DIMENSIONS: MILLIMETERS.

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