## MOSFET GATE DRIVER

The DRF200 drives up to 3nF gate capacitance of RF MOSFETs to frequencies over 15 MHz or 30 MHz into $50 \Omega$. The output rise and fall times are 10 ns , into $50 \Omega$, 15 n into $3 \mathrm{nF}+50 \Omega$. The DRF200 can deliver 100 W of output power. In addition the Driver provides an Anti-Ring function which limits output ringing at turn-on and turn-off of the power MOSFET. These attributes allow the device to be used in a wide variety of RF applications.


## Features

- Switching Frequency DC to $30 \mathrm{MHz} 50 \Omega$ Load
- Switching Frequency DC 15MHz 3nF Load
- Switching Speeds $10 n s 50 \Omega$, $15 n$ 3nF Load
- Low Pulse Width Distortion, $\leq 2 \%$
- Single Power Supply
- 1V CMOS Schmitt Trigger Input ~1V Hysteresis
- Current Output 12A Pk 8A RMS
- Power Dissipation Capability 100W
- RoHS compliant


## Typical Applications

- MOSFET Drivers
- RF Generators
- Switch Mode Power Amplifiers
- Digital Output Amplifiers
- Pulse Generators
- Laser Diode Drivers
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators
- High Power Clock Drivers


## Absolute Maximum Ratings

| Symbol | Parameter | Ratings | Unit |
| :---: | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{DS}}$ | Supply Voltage | 18 | V |
| $\mathrm{~V}_{\mathrm{I}}$ | Signal Input Voltage | -.7 to +5.5 | V |
| $\mathrm{I}_{\mathrm{D}}$ | ${\text { Continuous Drain Current } @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}}_{8}^{8}$ | A |  |
| $\mathrm{I}_{\mathrm{DM}}$ | Pulsed Drain Current $^{1}$ | 12 | C |

## Specifications

| Symbol | Parameter | Ratings |  | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DS}}$ | Supply Voltage Typical Operating | 8 to 15 |  | V |
| $V_{\text {in }}$ | Signal Input Voltage | -. 7 to +5.5 |  | V |
| ID | Continuous Drain Current @ $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | 8 |  | A |
| $\mathrm{I}_{\mathrm{DM}}$ | Pulsed Drain Current | 12 |  |  |
| $\mathrm{I}_{\mathrm{DQ}}$ | Quiescent Current | <2 |  | ma |
| PConsumption | Watts $=\mathrm{C}_{0}+\mathrm{C}_{L} \times V_{\text {DS }}{ }^{2} \times \mathrm{F} \times \mathrm{D}_{\text {UTY }} \mathrm{C}_{\text {YCLE }}$ | 100 |  | W |
| C | Output Capacitance | 2500 |  | pF |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance | 3 |  | pF |
| $\mathrm{R}_{\text {IN }}$ | Input Parallel Resistance | $\cong 1$ |  | $\mathrm{M} \Omega$ |
| Lout | Output Inductance | 3 |  | nH |
| $\mathrm{R}_{\text {OUt }}$ | Output Series Resistance | ~1 |  | $\Omega$ |
| $\mathrm{V}_{\text {IN (Low) }}$ | Input Low | 1.1 |  | V |
| $\mathrm{V}_{\text {IN (HIGH) }}$ | Input High | 1.9 |  | V |
|  | Test Conditions V ${ }_{\text {DS }}=15 \mathrm{~V}$ | RL=50 $\Omega$ | $\mathrm{CL}=2.5 \mathrm{nF}$ |  |
| Tr | Rise Time ( $10 \%$ to $90 \% \Delta \mathrm{~V}_{\text {Out }}$ ) | 10 | 15 | ns |
| Tf | Fall Time ( $90 \%$ to $10 \% \Delta \mathrm{~V}_{\text {Out }}$ ) | 10 | 15 | ns |


| $\mathrm{T}_{\mathrm{DLY}(\mathrm{ON})}$ | Throughput Delay | $30 \pm 3$ | ns |
| :---: | :--- | :---: | :---: |
| $\mathrm{~T}_{\mathrm{DLY}(\mathrm{OFF})}$ | Throughput Delay | $23 \pm 2$ | ns |
|  | Symmetry | 1.5 | $\%$ |
| $\mathrm{~F}_{\mathrm{MAXCL}}$ | $\mathrm{CL}=3 \mathrm{nF}+50 \Omega$ | 15 | MHz |
| $\mathrm{F}_{\mathrm{MAXRL}}$ | $\mathrm{RL}=50 \Omega$ | 30 | MHz |

## Thermal and Mechanical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{P}_{\mathrm{D}}$ | Total Power Dissipation @ $\mathrm{T}_{\mathrm{HS}}=25^{\circ} \mathrm{C}$ |  | 100 |  | W |
| $\mathrm{P}_{\mathrm{DC}}$ | Total Power Dissipation @ $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ |  | 170 |  | W |
| $\mathrm{R}_{\text {өjc }}$ | Junction to Case Thermal Resistance |  | . 88 |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {өJHS }}$ | Junction to Sink Thermal Resistance, Flat, Greased Surface |  | 1.38 |  |  |
| $\mathrm{T}_{\mathrm{J},}, \mathrm{T}_{\text {STG }}$ | Maximum Operating Junction Temperature |  |  | +175 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{J},}, \mathrm{T}_{\text {STG }}$ | Storage Junction Temperature Range | -55 |  | +150 | ${ }^{\circ} \mathrm{C}$ |

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Figure 1 Driver Circuit
A Simplified Driver IC circuit diagram is illustrated in Figure 1. The DRF200 Anti-Ring function is always on and the Invert, Non-Invert function is in the Non-invert mode. This function is not accessible in the DRF200. VIN is the control input Signal and it is paired with SG, the signal ground. This configuration provides a Kelvin signal connection to preserve control signal purity. The Driver has internal ESD protection, however good ESD practices should still be used when handling the device. U1 is a Schmitt Trigger Circuit; U2 provides the drive for U3. U3 is a power driver.


Figure 2 Driver Test Circuit
Figure 2 illustrates the Test Circuit for the DRF200. A 5 V signal is applied to the VIN and SG. +15 V is applied to Pin 4 ( $+V d s$ ) Pin 3 (GND) is attached the common ground. VOUT is measured at the Output Pin 5, across the RL and the CL, shown. All electrical data for this device is generated with the circuit of Figure 2.


Figure 3 DRF200 Mechanical Outline
Referring to Figure 3, the GND pin is the circuit ground for the +VDS supply and the output. No isolating Pad is required for mounting.

